OUTPUT CIRCUIT AND METHOD FOR REDUCING SIMULTANEOUS SWITCHING OUTPUT SKEW

ABSTRACT OF THE DISCLOSURE

An output circuit for outputting data with reduced simultaneous switching output skew includes N counts of output buffers and a comparator. The N counts of output buffers receive N counts of bit signals, respectively. At least one of the output buffers includes a delay unit for processing one of the bit signals into a delayed bit signal with an adjustable delay period in response to a delay signal, a pull-up unit electrically connected to the delay unit and a source voltage, and selectively enabled to output the delayed bit signal as a high level, and a pull-down unit electrically connected to the delay unit and a ground voltage, and selectively enabled to output the delayed bit signal as a low level. The comparator is electrically connected to the N counts of output buffers, compares the N counts of bit signals sampled at a first time spot and a second time spot, and generates the delay signal according to the comparing result.